USB3317

Hi-Speed USB Transceiver with 1.8V-3.3V ULPI Interface - 26MHz Reference Clock

PRODUCT FEATURES

Data Brief

- USB-IF “Hi-Speed” compliant to the Universal Serial Bus Specification Rev 2.0
- Interface compliant with the ULPI Specification revision 1.1 as a Single Data Rate (SDR) PHY
- 1.8V to 3.3V IO Voltage (±10%)
- flexPWR™ Technology
  - — Low current design ideal for battery powered applications
  - — “Sleep” mode tri-states all ULPI pins and places the part in a low current state
- Supports FS pre-amble for FS hubs with a LS device attached (UTMI+ Level 3)
- Supports HS SOF and LS keep-alive pulse
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 1.0a specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Allows host to turn VBUS off to conserve battery power in OTG applications
- Support OTG monitoring of VBUS levels with internal comparators
- “Wrapper-less” design for optimal timing performance and design ease
  - — Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- 26MHz Reference Clock Operation
  - — 0 to 3.6V input drive tolerant
  - — Able to accept “noisy” clock sources
- Internal low jitter PLL for 480MHz Hi-Speed USB operation
- Internal detection of the value of resistance to ground on the ID pin
- Integrated battery to 3.3V LDO regulator
  - — 2.2uF bypass capacitor
  - — 100mV dropout voltage
- Integrated ESD protection circuits
  - — Up to ±15kV without any external devices
- Carkit UART mode for non-USB serial data transfers
- Industrial Operating Temperature -40°C to +85°C
- Packaging Options
  - — 24 pin QFN lead-free RoHS compliant package (4 x 4 x 0.90 mm height)
  - — 25 ball VFBGA lead-free RoHS compliant package also available; (3 x 3 x 0.88mm height)

Applications

The USB3317 is targeted for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

The USB3317 is well suited for:

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- Set Top Boxes
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles
- POS Terminals

Order Number(s):

USB3317C-CP-TR FOR 24 PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE (TAPE AND REEL)

USB3317C-GJ-TR FOR 25 PIN, VFBGA LEAD-FREE ROHS COMPLIANT PACKAGE (TAPE AND REEL)

REEL SIZE IS 4000 PIECES.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

General Description

The USB3317 is a highly integrated Hi-Speed USB 2.0 Transceiver (PHY) that supports systems architectures based on a 26MHz reference clock. It is designed to be used in both commercial and industrial temperature applications.

The USB3317 meets all of the electrical requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) device. In addition to the supporting USB signaling the USB3317 also provides USB UART mode.

USB3317 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the Link. The industry standard ULPI interface uses a method of in-band signaling and status byte transfers between the Link and PHY, to facilitate a USB session. By using in-band signaling and status byte transfers the ULPI interface requires only 12 pins.

The USB3317 uses SMSC's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. SMSC's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

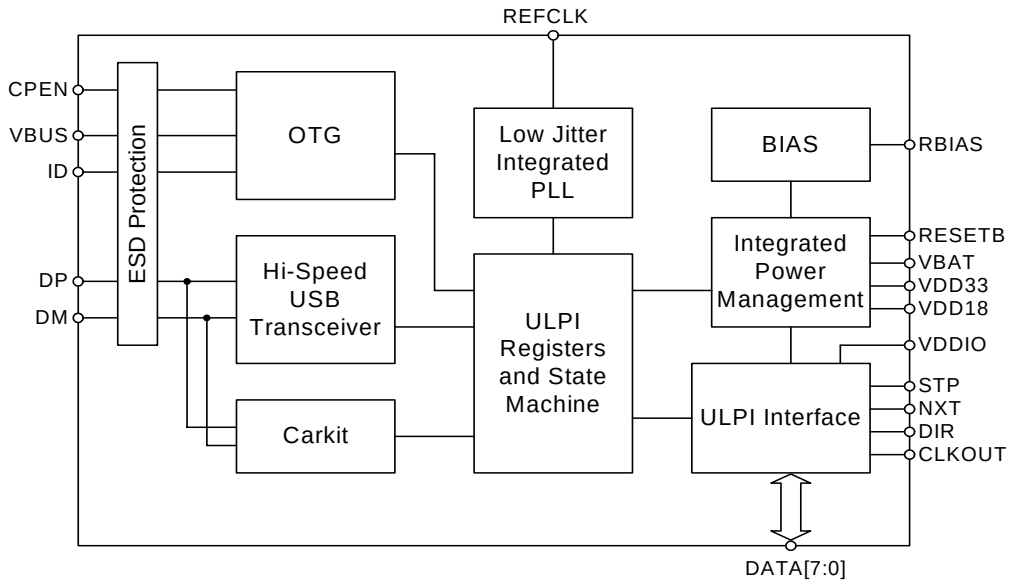


Figure 1 USB3317 Block Diagram

The USB3317 is designed to run with a 26MHz reference clock. By using a reference clock from the Link the USB3317 is able to remove the cost of a crystal reference from the design.

The USB3317 includes a integrated 3.3V LDO regulator to generate its own supply from power applied at the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.1 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.1V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. If the user would like to provide a 3.3V supply to the USB3317, the **VBAT** and **VDD33** pins should be connected together.

The USB3317 also includes integrated pull-up resistors that can be used for detecting the attachment of a USB Charger. By sensing the attachment to a USB Charger, a product using the USB3317 can charge its battery at more than the 500mA allowed when charging from a USB Host.

USB3317 Pin Locations and Descriptions

Package Diagram with Pin Locations

The pinout below is viewed from the top of the package.

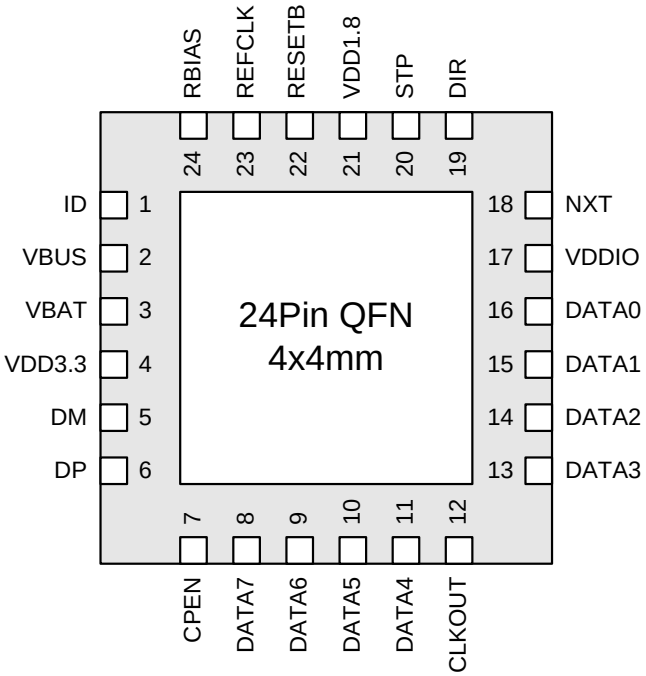


Figure 2 USB3317 QFN Pinout - Top View

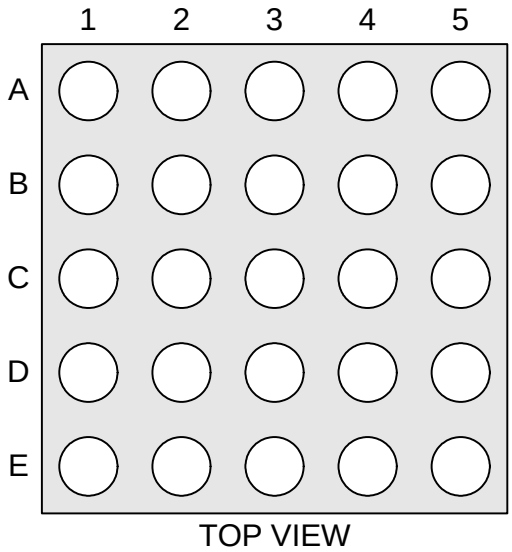


Figure 3 USB3317 VFBGA Pinout - Top View

Pin Definitions

The following table details the pin definitions for the figure above.

Table 1 USB3317 Pin Description

PIN BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
1 B1	**ID**	Input, Analog	N/A	**ID** pin of the USB cable. For non-OTG applications this pin can be floated. For an A-Device **ID** is grounded. For a B-Device **ID** is floated.
2 C1	**VBUS**	I/O, Analog	N/A	**VBUS** pin of the USB cable. This pin is used for the Vbus comparator inputs and for Vbus pulsing during session request protocol.
3 C2	**VBAT**	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.1V.
4 D2	**VDD3.3**	Power	N/A	3.3V Regulator Output. A 2.2uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3317.
5 D1	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
6 E1	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
7 E2	**CPEN**	Output, CMOS	High	External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The **CPEN** pin is low on POR. This pad uses VDD3.3 logic level.
8 E3	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
9 D3	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
10 E4	**DATA[5**	I/O, CMOS	N/A	ULPI bi-directional data bus.
11 D4	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
12 E5	**CLKOUT**	Output, CMOS	N/A	60MHz reference clock output. All ULPI signals are driven synchronous to the rising edge of this clock.
13 D5	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
14 C4	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.

Table 1 USB3317 Pin Description (continued)

PIN BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
15 C5	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
16 B4	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
17 B5	**VDDIO**	Power	N/A	1.8V to 3.3V ULPI interface supply voltage. This voltage sets the value of V_{OH} for the ULPI interface.
18 A5	**NXT**	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY. The Link places the next byte on the data bus in the following clock cycle.
19 A4	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
20 A3	**STP**	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
21 B3	**VDD1.8**	Power	N/A	External 1.8V Supply input pin. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB3317.
22 B2	**RESETB**	Input, CMOS,	N/A	When low, the part is suspended with all of the I/O tri-stated. When high the USB3317 will operate as a normal ULPI device.
23 A2	**REFCLK**	Input, CMOS	N/A	26MHz Reference Clock input.
24 A1	**RBIAS**	Analog, CMOS	N/A	Rbias pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB3317.
FLAG C3	**GND**	Ground	N/A	Ground. QFN only: The flag should be connected to the ground plane with a via array under the exposed flag. This is the main ground for the IC.

Application Diagrams

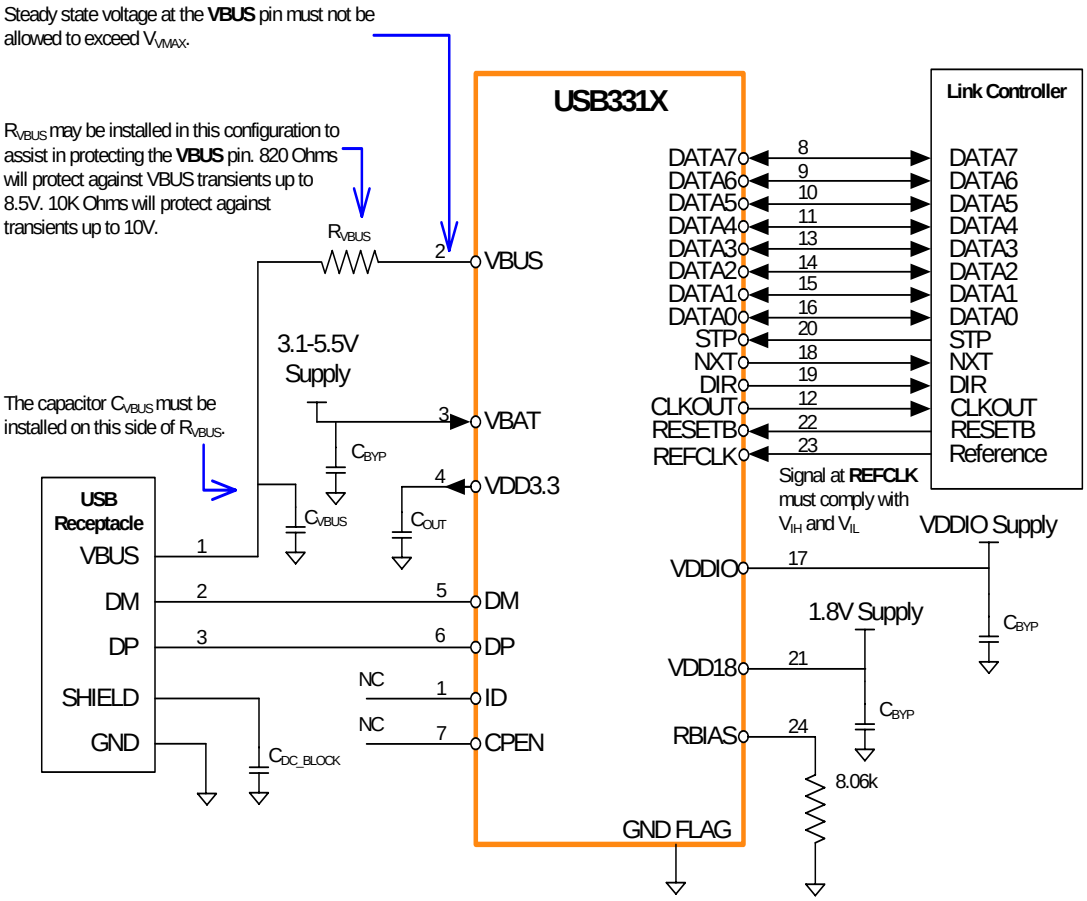


Figure 4 USB3317 QFN Application Diagram (Device)

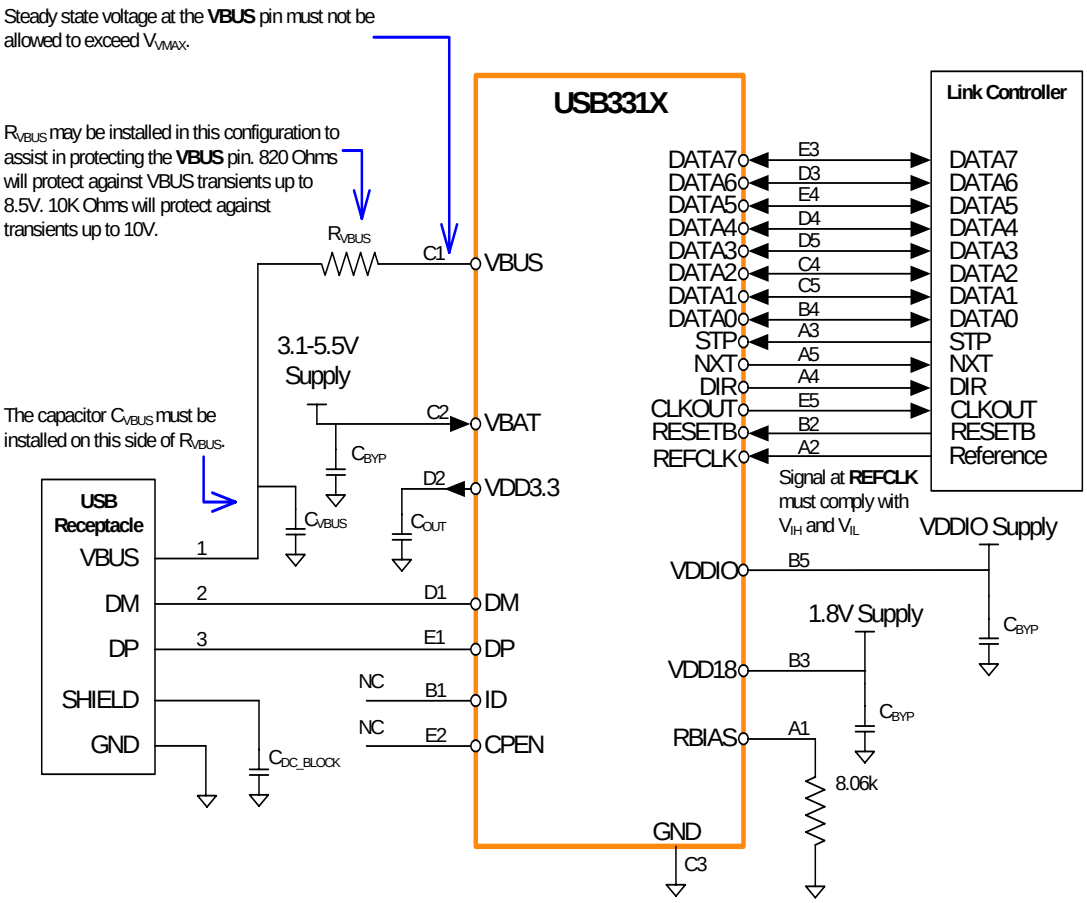


Figure 5 USB3317 VFBGA Application Diagram

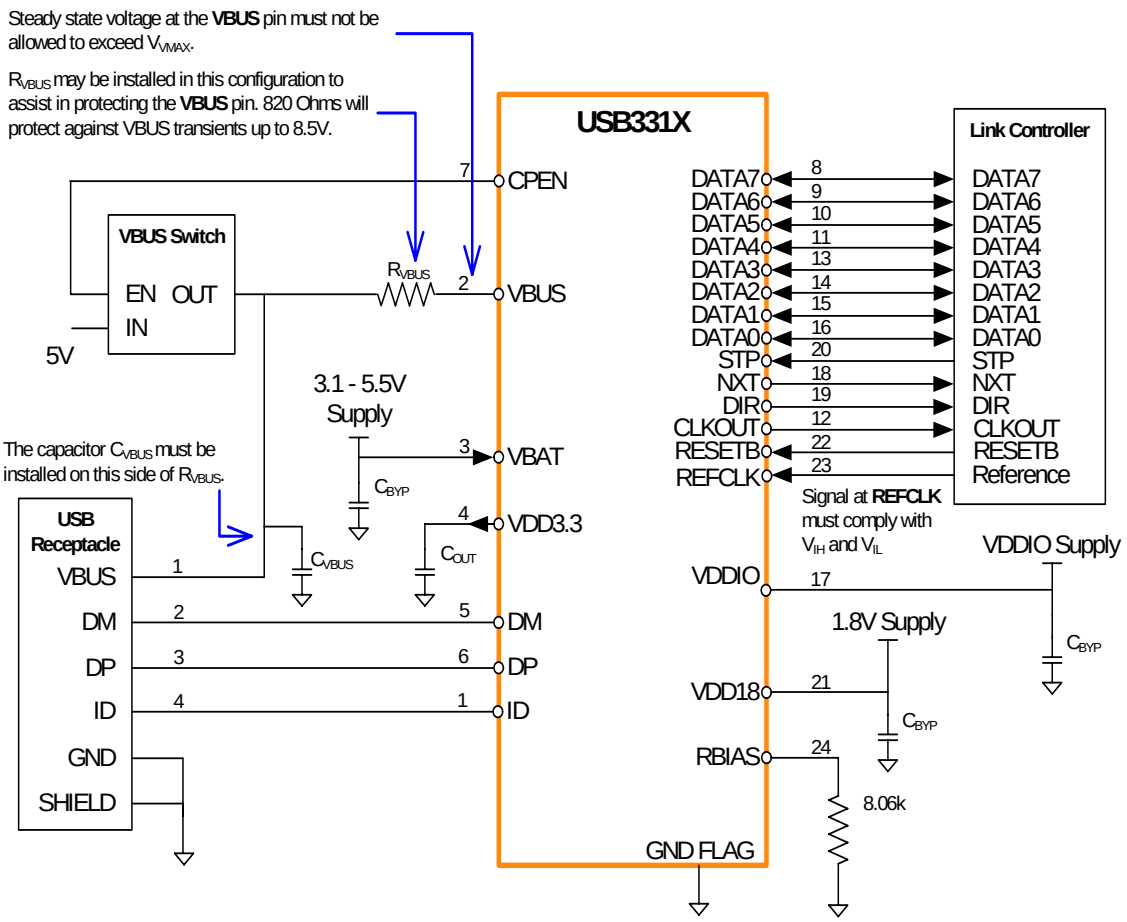
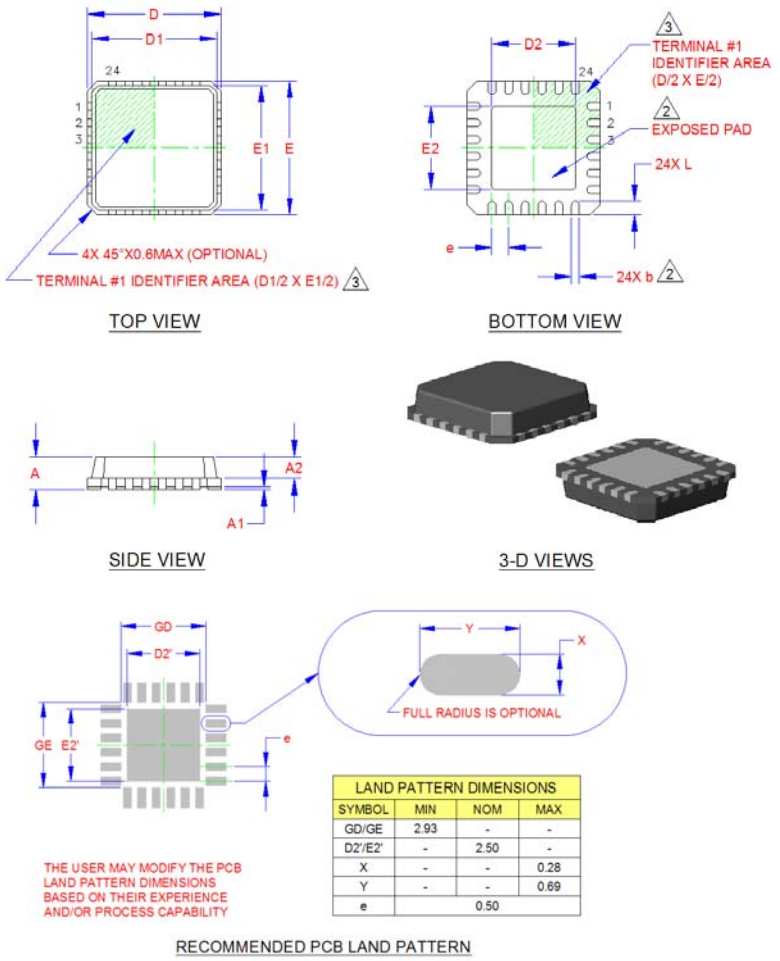


Figure 6 USB3317 QFN Application Diagram (Host or OTG)

Package Outlines

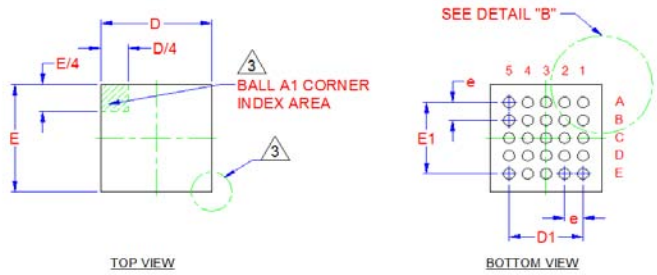


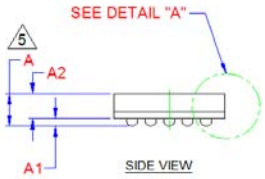
LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.93	-	-
D2'/E2'	-	2.50	-
X	-	-	0.28
Y	-	-	0.69
e		0.50	

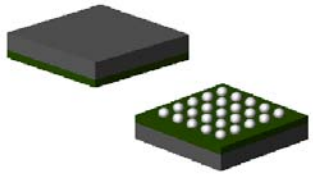
COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	-	0.90	-	MOLD CAP THICKNESS
D/E	3.85	4.00	4.15	-	X/Y BODY SIZE
D1/E1	3.55	-	3.95	-	X/Y MOLD CAP SIZE
D2/E2	2.40	2.50	2.60	2	X/Y EXPOSED PAD SIZE
L	0.30	-	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			-	TERMINAL PITCH

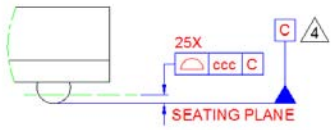
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

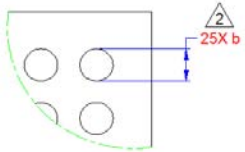
Figure 7 24-Pin QFN, 4x4mm Body, 0.5mm Pitch

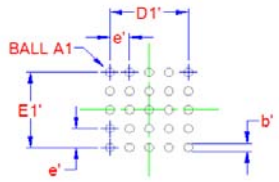












LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1'/E1'	-	2.00	-
b'	0.20	-	0.25
e'	-	0.50	-

THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

RECOMMENDED PCB LAND PATTERN

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	-	-	1.00	5	OVERALL PACKAGE HEIGHT
A1	0.15	-	-	-	STANDOFF
A2	0.65	-	-	-	PKG BODY THICKNESS
D/E	2.90	3.00	3.10	-	X/Y BODY SIZE
D1/E1		2.00 BSC		-	X/Y END BALLS DISTANCE
b	0.25	0.30	0.35	2	BALL DIAMETER
e		0.50 BSC		-	BALL PITCH
ccc	0	-	0.08	4	COPLANARITY

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAXIMUM RADIAL TRUE POSITION TOLERANCE OF EACH BALL IS ± 0.075mm AT MAXIMUM MATERIAL CONDITION. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM "C".
3. THE BALL "A1" CORNER MUST BE IDENTIFIED IN THE INDICATED AREA OF THE TOP PACKAGE SURFACE BY USING A CORNER CHAMFER, INK/LASER/METALIZED MARKING, INDENTATION, OR OTHER FEATURE OF PACKAGE BODY. EXACT SHAPE OF EACH CORNER IS OPTIONAL, BUT TERMINAL "A1" CORNER MUST BE UNIQUE.
4. PRIMARY DATUM "C" AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT SOLDER BALLS.
5. DIMENSION "A" DOES NOT INCLUDE ATTACHED EXTERNAL FEATURES, SUCH AS HEAT SINK OR CHIP CAPACITORS.

Figure 8 25-pin VFBGA, 3x3mm Body, 0.5mm Pitch